19-6310; Rev 0; 5/12

EVALUATION KIT AVAILABLE

MAX14627/MAX14628

Low-Power Headset Detectors with SEND/END Button Support

General Description

The MAX14627/MAX14628 provide a simple solution for detecting the insertion and managing the operation of a 3.5mm stereo headset with a microphone. These devices integrate all circuitry needed to detect SEND/END button press events and generate required microphone bias voltages, and are fully compatible with Windows Mobile 7.

The devices need only three GPIOs from the host controller to select between call mode and standby mode, and monitor the SEND/END and jack insertion status. In call mode, the low-noise LDO is enabled to provide DC bias to the externally preamplified microphone. In standby mode, microphone low-power pulsing is enabled to reduce supply current while waiting for a SEND/END button press event. Two open-drain outputs signal the host controller when an insertion/removal or SEND/END button press event occurs. If a 3P headset without a microphone is inserted, the low-power pulsing can be disabled by setting the MODE input to high impedance.

The MAX14627 operates from a 2.5V to 5.5V input voltage supply and features an internal 2.2V LDO output, while the MAX14628 operates from a 3.1V to 5.5V voltage supply and features an internal 2.8V LDO output voltage. Both devices control jack insertion detection by monitoring a 3.5mm socket with a normally open jack insertion switch. Additionally, the MAX14628 features open microphone detection.

The MAX14627/MAX14628 are available in an 8-pin TDFN package, and are fully specified over the -40°C to +85°C extended temperature range.

Benefits and Features

- **Versatile Jack Detection and Control**
  - **MODE Three-State Microphone Bias Control**
  - **MIC Switch Ground Detection (MAX14627)**
  - **MIC Switch Open and Ground Detection (MAX14628)**
- **Compatible with Windows Mobile 7 and Google Android**
  - **Microphone Button Press Detection**
- **High-Performance MIC Bias and Power Savings**
  - **No Pop-Up Noises**
  - **Ultra-Low Noise, High-PSRR MIC Bias**
  - **Low-Power MIC Idle Mode**
  - **Automatic Ultra-Low-Power Mode When Microphone Is Disabled**
- **PCB Space and Cost Savings**
  - **Integrated ±15kV ESD Protection (HBM) on DETIN and MIC Input Terminals**
  - **Small 8-Pin (2mm x 2mm) TDFN Package**

Applications

Cell Phones

Portable Media Players

Tablet/Laptop PCs

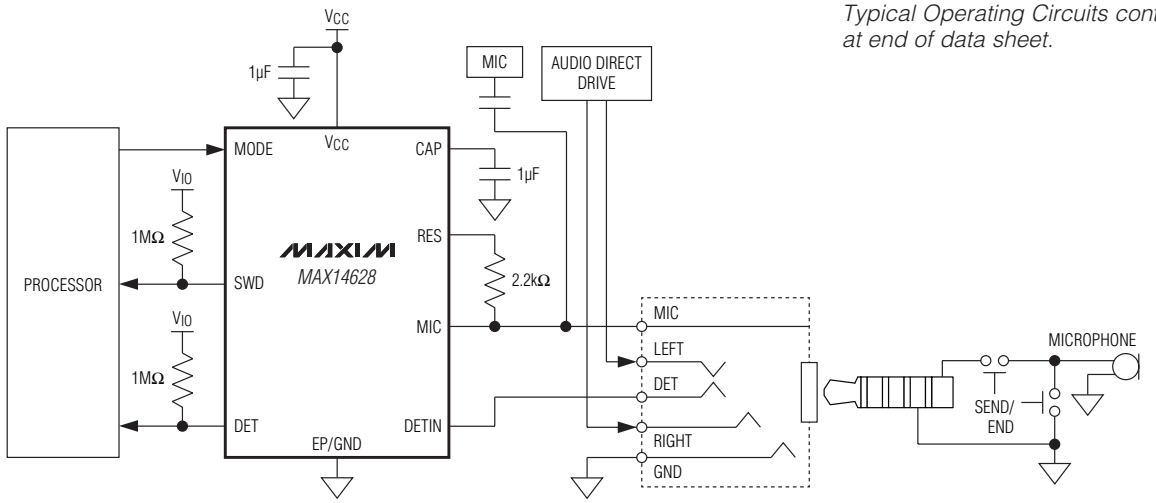
***Ordering Information* appears at end of data sheet.**

*For related parts and recommended products to use with this part, refer to **www.maxim-ic.com/MAX14627.related**.*

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Typical Operating Circuits

Typical Operating Circuits continued at end of data sheet.



For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

ABSOLUTE MAXIMUM RATINGS

(Voltages referenced to GND.)
V_{CC}, MODE, SWD, DET .....-0.3V to +6V
CAP, MIC, RES..... -0.3V to (V_{CC} + 0.3V)
DETIN .....-6V to +6V
Continuous Current into Any Terminal ..... ±100mA
Continuous Power Dissipation (T_A = +70°C)
TDFN (derate 11.9mW/°C above +70°C).....953.5mW

Operating Temperature Range ..... -40°C to +85°C
Junction Temperature .....+150°C
Storage Temperature Range..... -65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow) .....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PACKAGE THERMAL CHARACTERISTICS (Note 1)

TDFN
Junction-to-Ambient Thermal Resistance (θ_{JA}) .....83.9°C/W
Junction-to-Case Thermal Resistance (θ_{JC}).....37°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maxim-ic.com/thermal-tutorial**.

ELECTRICAL CHARACTERISTICS

(V_{CC} = 2.5V to 5.5V for MAX14627, V_{CC} = 3.1V to 5.5V for MAX14628, C_{DETIN} < 100pF, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +3.6V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DC CHARACTERISTICS							
Supply Voltage Range	V_{CC}	MAX14627		2.5		5.5	V
		MAX14628		3.1		5.5	
V_{CC} Undervoltage-Lockout Threshold	V_{CCUVLO}	V_{CC} rising		0.9	1.7	2.45	V
V_{CC} Supply Current	I_{CC}	MAX14627, V_{CC} = 2.8V	MODE = low, DETIN = high			1.3	µA
			MODE = low, DETIN = low, I_{MIC} = 300µA			11.7	
			MODE = high, DETIN = low, I_{MIC} = 300µA			800	
			MODE = high-Z, DETIN = low			6.0	
		MAX14628, V_{CC} = 3.3V	MODE = low, DETIN = high			1.9	
			MODE = low, DETIN = low, I_{MIC} = 300µA			13.2	
			MODE = high, DETIN = low, I_{MIC} = 300µA			800	
			MODE = high-Z, DETIN = low			7.0	

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 2.5V to 5.5V for MAX14627, V_{CC} = 3.1V to 5.5V for MAX14628, C_{DETIN} < 100pF, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +3.6V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DETIN Pullup Resistance	R_{DETIN}			1000		kΩ
DETIN Series Resistance	$R_{DETININT}$			100		kΩ
Negative Current from DETIN	I_{NDETIN}	V_{DETIN} = -2V			31	µA
MIC SEND/END Detection Threshold	V_{MICTH_LOW}		0.20 x V_{BIAS}	0.22 x V_{BIAS}	0.24 x V_{BIAS}	V
MIC Open Switch Detection Threshold	V_{MICTH_HI}	MAX14628	0.90 x V_{BIAS}	0.94 x V_{BIAS}	0.98 x V_{BIAS}	V
DETIN Detection Threshold	$V_{DETINTH}$	Falling edge	1/3 x V_{CC}	1/2 x V_{CC}	2/3 x V_{CC}	V
MODE Pullup Resistance for High-Z Detection	R_{MODE_HI}			200		kΩ
MODE Pulldown Resistance for High-Z Detection	R_{MODE_LO}			200		kΩ
LINEAR REGULATOR (CAP)						
Output Current Limit	I_{CAP}	V_{CAP} = 0V	4			mA
LDO Output Voltage	V_{LDO}	MAX14627, V_{CC} = 2.8V	2.0	2.2	2.45	V
		MAX14628, V_{CC} = 3.3V	2.55	2.8	3.1	
LDO PSRR	$PSRR_{LDO}$	Noise from V_{CC} to CAP, f = 217Hz, V_{CC} = 2.8V ±0.1V, I_{CAP} = 300µA, MODE = high		100		dB
LDO Noise	N_{LDO}	V_{CC} = 2.8V, I_{MIC} = 300µA, f = 100Hz to 4000Hz		11		$µV_{RMS}$
LDO Turn-Off Time	t_{LDO_OFF}	MAX14627, V_{CC} = 2.8V, R_L = 2kΩ, V_{CAP} from 90% to 10%		60		µs
		MAX14628, V_{CC} = 3.3V, R_L = 2kΩ, V_{CAP} from 90% to 10%		60		
Minimum Bypass Capacitance	C_{OUT}	(Note 3)	0.22			µF
DIGITAL SIGNALS (MODE, SWD, DET)						
Input Logic-High Voltage	V_{IH}		1.4			V
Input Logic-Low Voltage	V_{IL}				0.4	V
MODE Average Current	I_{MODE_LOW}	Pulsing with 1/64 duty cycle from MODE terminal when MODE = low, DETIN = low (Note 4)			1	µA
MODE Input Resistance	R_{MODE_HI}	When MODE = high, DETIN = low	120	220	380	kΩ
MODE External Maximum Leakage	I_{MODE_LKG}	When MODE = high-Z (Note 3)	-1		+1	µA
Output Logic-High Leakage Current (Open Drain)	I_{OH_LKG}	V_{OH} = 5V			1	µA

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 2.5V to 5.5V for MAX14627, V_{CC} = 3.1V to 5.5V for MAX14628, C_{DETIN} < 100pF, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +3.6V, T_A = +25°C.) (Note 2)

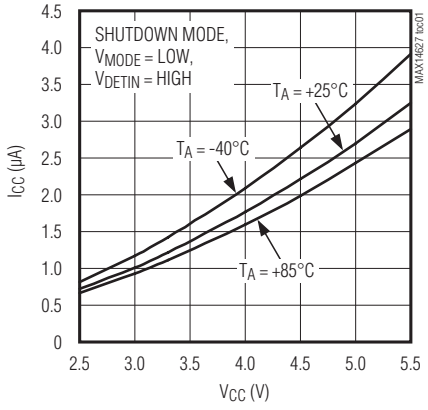
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Logic-Low Voltage	V_{OL}	I_{SINK} = 1mA			0.4	V
DYNAMIC CHARACTERISTICS						
MODE Maximum Load Capacitance	C_{MODE}	(Note 3)			200	pF
MIC Low-Power Mode On-Time	t_{MICLPO}			120		µs
MIC Low-Power Mode Period	t_{MICLPP}			8		ms
High-Z Detection Time	t_{HIZDET}			16		ms
MODE 0 → 1 Detection Time	$t_{MODE0-1}$			4		ms
MODE 1 → 0 Detection Time	$t_{MODE1-0}$			16		ms
DETIN Debounce Time	t_{DIDEB}	Falling edge		300		ms
SEND/END Debounce Time	t_{SEDEB}			30		ms
ESD PROTECTION						
MIC, DETIN		Human Body Model		±15		kV
All Other Pins		Human Body Model		±2		kV

Note 2: All devices are production tested at T_A = +25°C. Specifications over temperature are guaranteed by design.
Note 3: External specification requirements.
Note 4: Guaranteed by design.

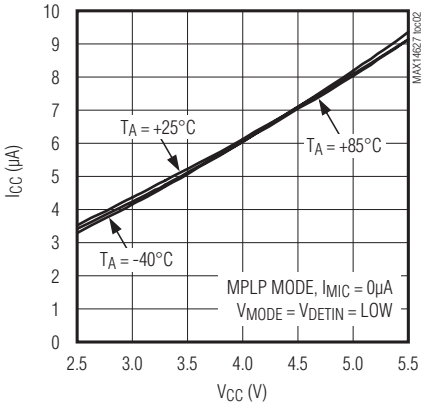
Typical Operating Characteristics

(V_{CC} = 3.3V, T_A = +25°C, C_{DETIN} < 100pF, unless otherwise noted.)

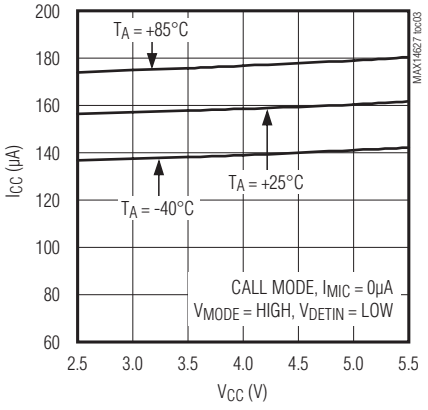
VCC SUPPLY CURRENT vs. VOLTAGE



VCC SUPPLY CURRENT vs. VOLTAGE



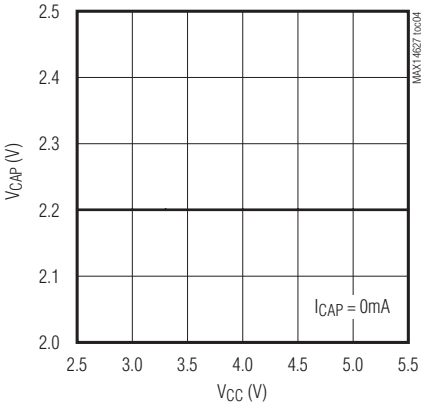
VCC SUPPLY CURRENT vs. VOLTAGE



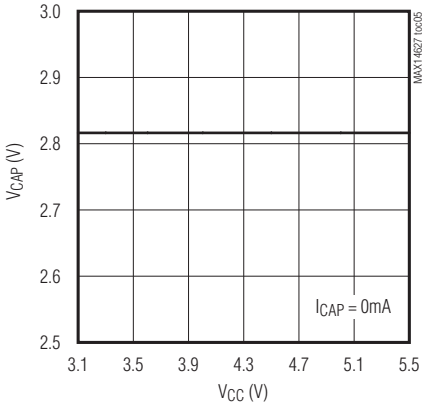
Typical Operating Characteristics (continued)

(V_{CC} = 3.3V, T_A = +25°C, C_{DETIN} < 100pF, unless otherwise noted.)

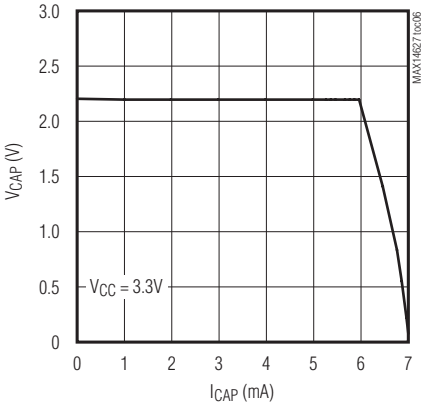
MAX14627 CAP VOLTAGE vs. V_{CC}



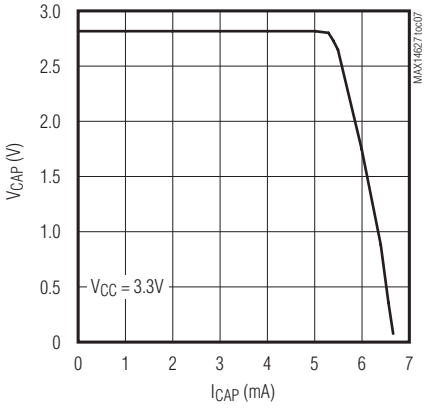
MAX14628 CAP VOLTAGE vs. V_{CC}



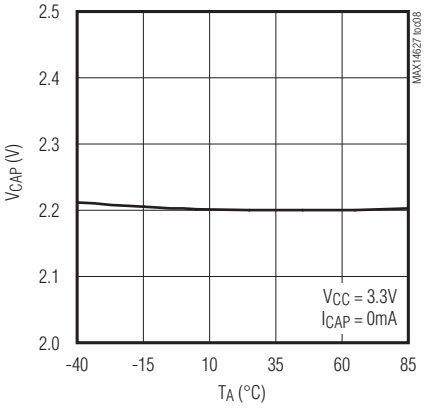
MAX14627 CAP VOLTAGE vs. CURRENT



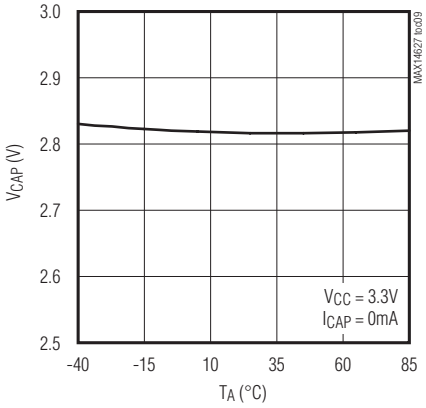
MAX14628 CAP VOLTAGE vs. CURRENT



MAX14627 CAP VOLTAGE vs. TEMPERATURE



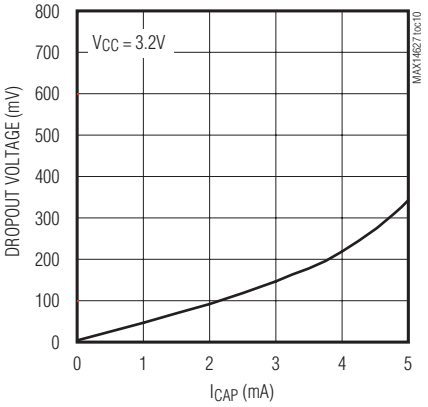
MAX14628 CAP VOLTAGE vs. TEMPERATURE



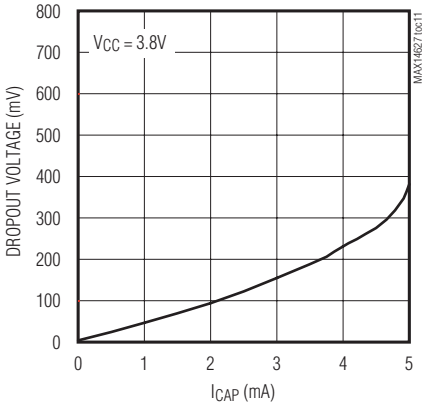
Typical Operating Characteristics (continued)

(V_{CC} = 3.3V, T_A = +25°C, C_{DETIN} < 100pF, unless otherwise noted.)

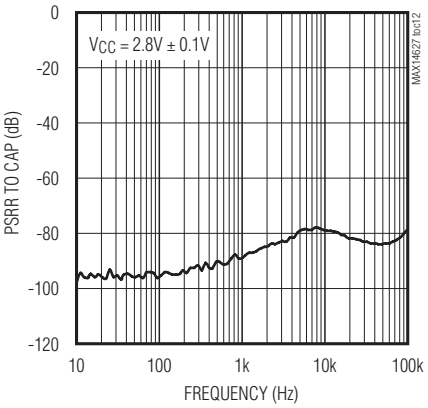
MAX14627 CAP DROPOUT VOLTAGE vs. CAP CURRENT



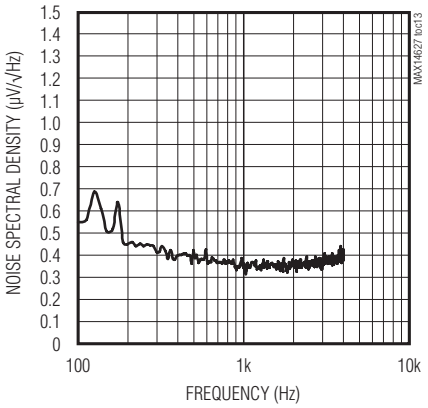
MAX14628 CAP DROPOUT VOLTAGE vs. CAP CURRENT



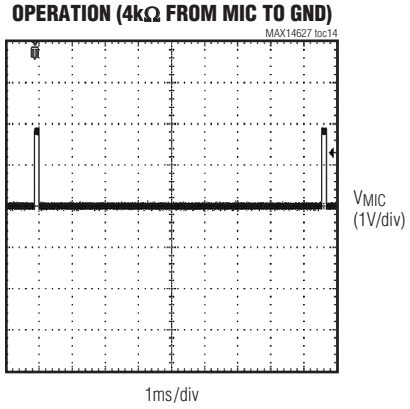
CAP POWER SUPPLY REJECTION RATIO vs. FREQUENCY



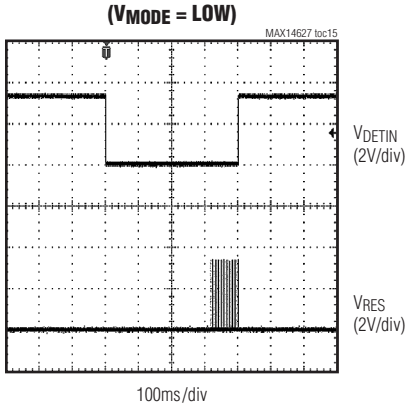
CAP NOISE DENSITY vs. FREQUENCY



MICROPHONE LOW-POWER MODE OPERATION (4kΩ FROM MIC TO GND)



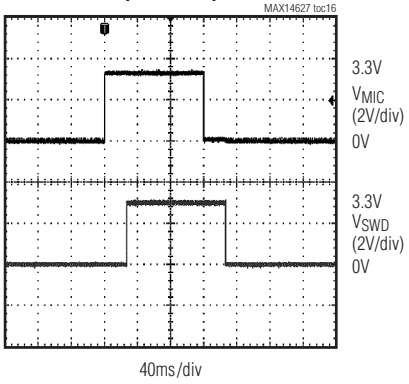
DETIN DEBOUNCE TIMING (V_{MODE} = LOW)



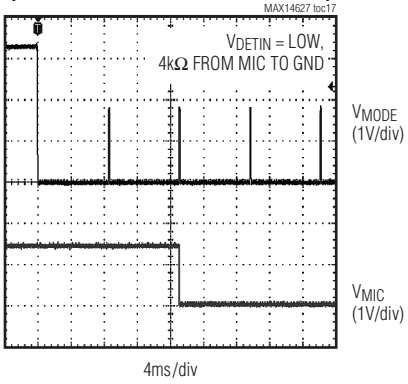
Typical Operating Characteristics (continued)

(V_{CC} = 3.3V, T_A = +25°C, C_{DETIN} < 100pF, unless otherwise noted.)

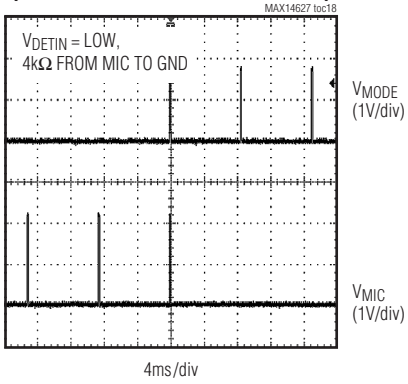
SWD DEBOUNCE TIMING (MODE = L)



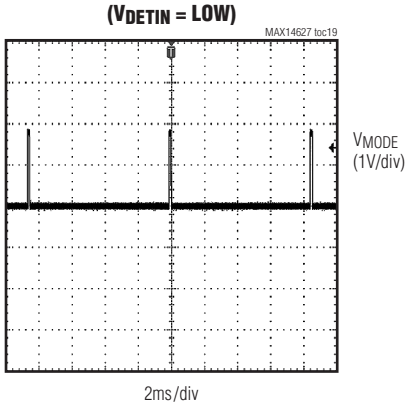
MIC vs. MODE (TRANSITIONS FROM HIGH TO HIGH-Z)



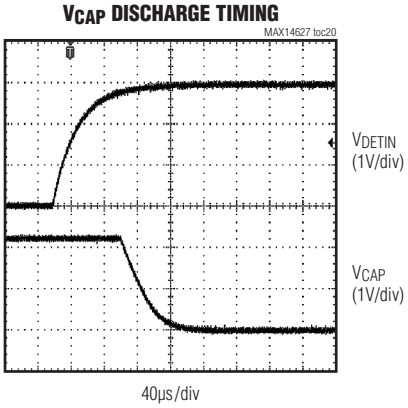
MIC vs. MODE (TRANSITIONS FROM LOW TO HIGH-Z)



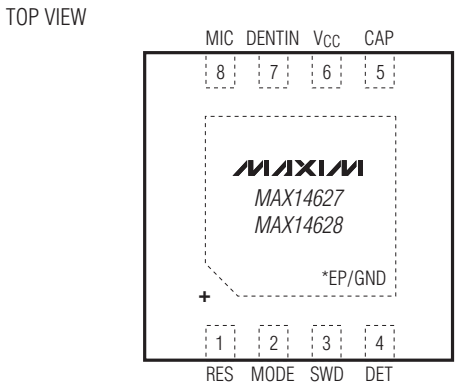
MODE PULSING IN HIGH-Z (V_{DETIN} = LOW)



V_{CAP} DISCHARGE TIMING



Pin Configuration



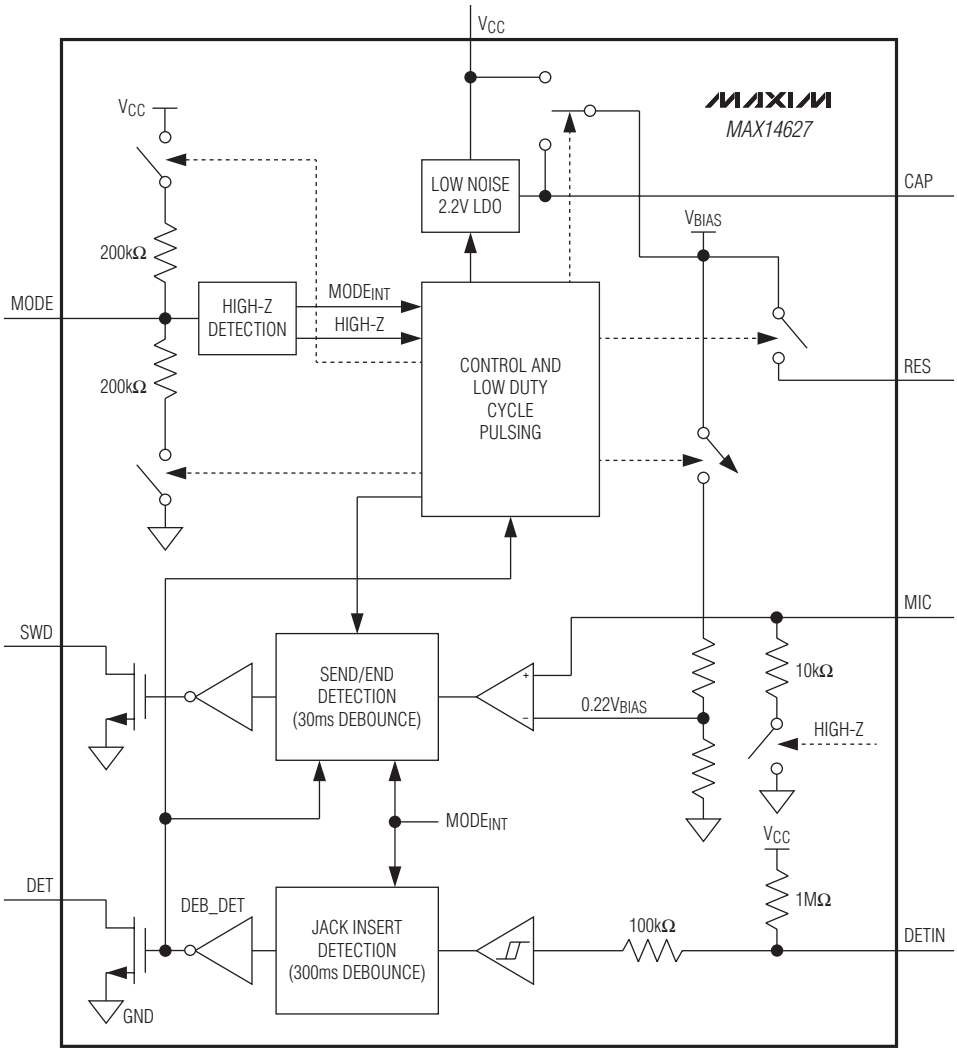
TDFN

*CONNECT THE EXPOSED PAD (EP/GND) TO THE GROUND PLANE.

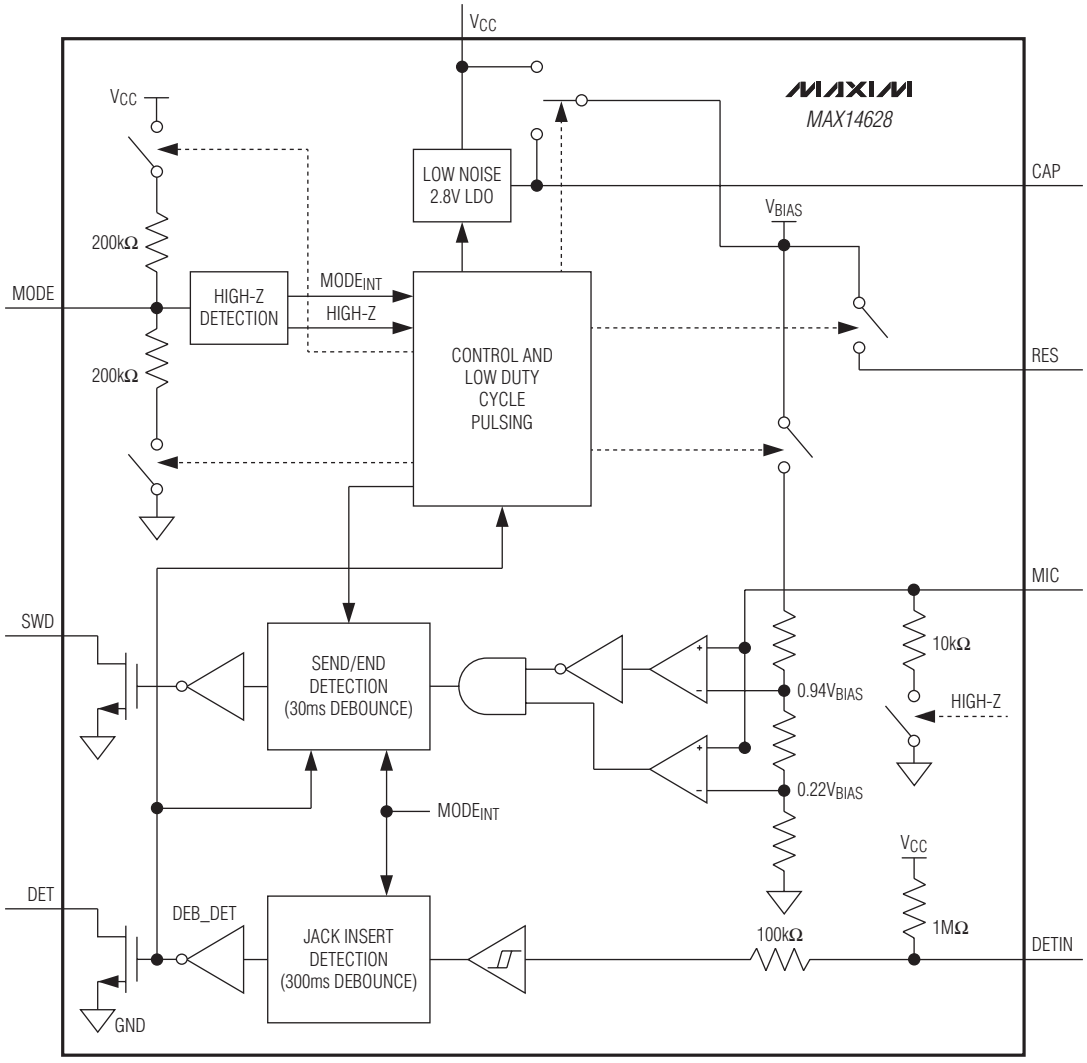
Pin Description

PIN	NAME	FUNCTION
1	RES	Resistor Connection. Connect an external 2.2kΩ resistor from RES to MIC for microphone biasing.
2	MODE	Microphone Mode Selection Three-State Input. MODE selects the operating mode. See the *MODE Control Input* section for more information.
3	SWD	SEND/END Button Detection Output. SWD is an active-low, open-drain output.
4	DET	Jack Insertion Detection Output. DET is asserted when there is a 3.5mm jack inserted into the socket. DET is an active-low open-drain output.
5	CAP	Internal LDO Output. Connect a 1µF ceramic (X5R, X7R, or better) capacitor between CAP and ground as close as possible to the device.
6	V_{CC}	Supply Voltage Input. Bypass V_{CC} to ground with a 1µF ceramic capacitor as close as possible to the device.
7	DETIN	Jack Insertion Detection Input. An internal comparator monitors DETIN for jack insertion/removal events.
8	MIC	Microphone Connection Input. An internal comparator monitors MIC for SEND/END button press events.
—	EP/GND	Exposed Pad. The exposed pad is the ground connection for the device. Connect EP/GND to the ground plane.

MAX14627 Functional Diagram



MAX14628 Functional Diagram



Detailed Description

The MAX14627/MAX14628 manage headsets by integrating 3.5mm jack insertion detection, microphone bias generation, and SEND/END button press detection. Both devices feature a low-power microphone mode to reduce the high bias current required for microphone operation while it is not in use. These devices require only a single three-state input (MODE) to select between call mode and two different low-power modes. See the *Internal LDO Regulator* and *SEND/END Button Press Detection* sections for details about the differences between these two devices.

Internal LDO Regulator

The devices integrate a low-noise, low-dropout regulator (LDO) for biasing the microphone connected to MIC. The LDO output voltage is set at 2.2V for the MAX14627 and 2.8V for the MAX14628. The LDO is enabled and enters low-noise mode (LNM) when the MODE input is logic-high and a jack is detected (DETIN is low). Pull the MODE input low or leave it open to put the LDO in low-power shutdown mode (SDM).

Connect a 1µF capacitor from CAP to ground as close as possible to the pin.

Microphone Operation and Bias Voltage Generation

An externally preamplified microphone is connected to MIC. Connect MIC to RES through an external 2.2kΩ resistor to bias the microphone.

The devices generate a bias voltage (V_{BIAS}) at RES. V_{BIAS} is connected to the internal LDO when the LDO is on or connected to V_{CC} when the LDO is off.

Microphone Low-Power Mode (MPLP)

A microphone draws a large amount of current due to the 2.2kΩ required bias resistor when it is connected. This current is dissipated even when the microphone is not in use for audio input. This allows the SEND/END button detection to operate. The devices feature internal circuitry to reduce this current while simultaneously detecting SEND/END button press events.

When a jack is inserted (DETIN is low and DET is asserted low) and if MODE is pulled low, these devices enter the microphone low-power mode (MPLP). In this mode, MIC is periodically connected to V_{BIAS} (= V_{CC}) through the 2.2kΩ resistor to RES only for a short duration (120µs pulse over an 8ms period) to check for the SEND/END button press event (switch to GND in both MAX14627/MAX14628 and switch open in the MAX14628 only).

The devices exit MPLP when the MODE input transitions to logic-high or to high-Z state.

Note that V_{BIAS} is disconnected from RES when no jack is inserted and microphone low-power mode is not entered.

Jack Insertion Detection

The devices monitor the DETIN input to detect jack insertion/removal events. Debounce circuitry ensures that transient voltages do not force the device to enter or exit microphone low-power mode due to false jack insertion/removal detection. DETIN input is capable of handling ±15kV HBM ESD event.

The devices are designed for sockets with a normally open pin. Without the 3.5mm jack inserted at DETIN, the input is pulled high by a large internal pullup resistor (1MΩ). When the jack is plugged in, DETIN is pulled to ground through the detection pin of the jack. DET is then asserted (after 300ms debounce time) and MIC is biased according to the logic state of the MODE input as follows:

- If MODE is low, the external 2.2kΩ resistor connects MIC to V_{CC} in pulsing mode (MPLP) waiting for a SEND/END button press event.
- If MODE is high, the external 2.2kΩ resistor connects MIC to LDO output continuously.
- If MODE is high-Z, MIC is internally pulled down.

The devices feature an internal series 100kΩ resistor at DETIN and do not require a series resistor between DETIN and the jack even when a direct drive audio output is connected to DETIN through the detection pin of the jack. DETIN withstands input voltages down to -2V.

Ensure that the total capacitance on DETIN is less than 100pF.

SEND/END Button Press Detection

The devices monitor the MIC input to detect SEND/END button press events. The SEND/END button press with the 4P microphone headset is detected and pulls the SWD output low if the voltage at MIC falls below the MIC switch to GND detection threshold (0.22 x V_{BIAS}) for longer than 30ms.

The MAX14628 also features an additional SEND/END detection mechanism through an additional MIC switch open detection threshold (0.94 x V_{BIAS}). If there is an open switch, then MIC is pulled up to V_{BIAS} in pulsing mode. If this happens for longer than 30ms, then the output SWD is pulled low.

The debounce period built into the SEND/END button press detection allows the mechanical SEND/END button to reach steady-state before applying the microphone bias. This mitigates click-and-pop noise.

The SEND/END detection circuitry is active whenever a jack is inserted (DETIN is low and DET is low).

MODE High-Z State

If a 3P headset without a microphone is inserted, the SWD output is asserted low continuously. The user can turn off the microphone low-power mode by placing the MODE input to high-Z state after the recognition of a 3P jack. When in high-Z state, MODE is internally driven in pulsed mode.

MODE Control Input

An external host processor controls the MODE input. Table 1 shows the behavior of these devices based on the MODE input and jack insertion status. The device enters call mode when the MODE pin is logic-high and a jack is detected, enabling the LDO immediately in low-noise mode (LNM). The LDO output powers V_{BIAS} and is connected to the microphone (MIC) through the external 2.2kΩ bias resistor.

Drive MODE low to put the devices in standby mode. In standby mode, V_{CC} powers V_{BIAS}, the LDO enters shut-down mode (SDM), and the microphone bias connection either turns off permanently if no jack is inserted or enters MPLP if a jack is inserted.

When MODE is set to high-Z, both the LDO and MPLP turn off. Also, the SWD output returns to a high-Z state, which can be used as a feedback of the device.

The MODE input is designed to be compatible with 1.8V logic when the V_{CC} is up to 5.5V. The MODE pin must be properly controlled based on DETIN status to avoid the click-and-pop noise due to a headset insertion.

Applications Information

Typical Connections for 3.5mm Jacks

There are two typical 3.5mm jacks: tip-ring-ring-sleeve (TRRS) with four conductors (Figure 1a) and tip-ring-sleeve (TRS) with three conductors (Figure 1b). The most common configuration of the TRRS jack is to use rings 1 and 2 for audio signals, ring 3 for ground, and ring 4 for a microphone. The TRS jack typically uses rings 1 and 2 for audio signals and rings 3 and 4 as ground.

Supported Accessories

All the devices support all standard configurations of headsets with a microphone and SEND/END button on a TRS or TRRS 3.5mm jack. Figure 2 shows the supported connections of the speakers, SEND/END button, and microphone to the jack.

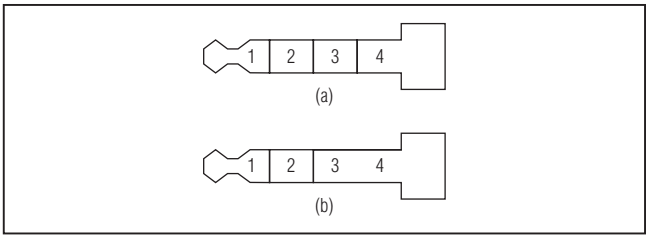


Figure 1. Typical 3.5mm Jacks

Table 1. Operating Modes

MODE	LOW		HIGH-Z		HIGH	
DETIN	Low	High	Low	High	Low	High
LDO Mode	SDM		SDM		LNM	SDM
MIC Bias Mode	MPLP	Off	Off*	Off	2.2kΩ	Off

**MIC is internally pulled down.*

Headset with No Microphone

When the 3.5mm jack in Figure 2a is inserted, the MIC input is pulled low permanently by the ground connection on the sleeve and the SWD output is logic-low permanently. This type of headset is supported by implementing a timeout period in software to recognize that the permanent SWD logic-low state is not due to a very long SEND/END button press event. In this case, the MODE input pin can be placed in high-Z state to disable the pulsing on the MIC pin (MPLP) and set the SWD output in high-Z state.

Headset with Microphone and Normally Open SEND/END Button in Parallel

When the 3.5mm jack in Figure 2b is inserted, the MIC input is pulled below the threshold only during a SEND/END button press event. The SWD output is logic-low when the SEND/END button is pressed for more than the 30ms (typ) debounce time.

Headset with Normally Open SEND/END Button and Resistive Remote Control

The devices support the 3.5mm jack with a microphone and two buttons in Figure 2c that is the standard Windows Mobile configuration. The threshold is set to detect a button press, regardless of which button is pressed.

Headset with Microphone and Normally Closed SEND/END Button in Series

The MAX14628 supports the 3.5mm jack with a microphone and a normally closed series switch. When the switch opens for more than the 30ms (typ) debounce time (SEND/END button press event), the SWD output asserts low.

High-ESD Protection

Electrostatic discharge (ESD)-protection structures are incorporated on all pins to protect against electrostatic discharges up to ±2kV Human Body Model (HBM) encountered during handling and assembly. DETIN and MIC are further protected against ESD up to ±15kV (HBM) without damage. After an ESD event, all the devices continue to function without latchup.

ESD Test Conditions

ESD performance depends on a variety of conditions. Contact Maxim for a reliability report that documents test setup, test methodology, and test results.

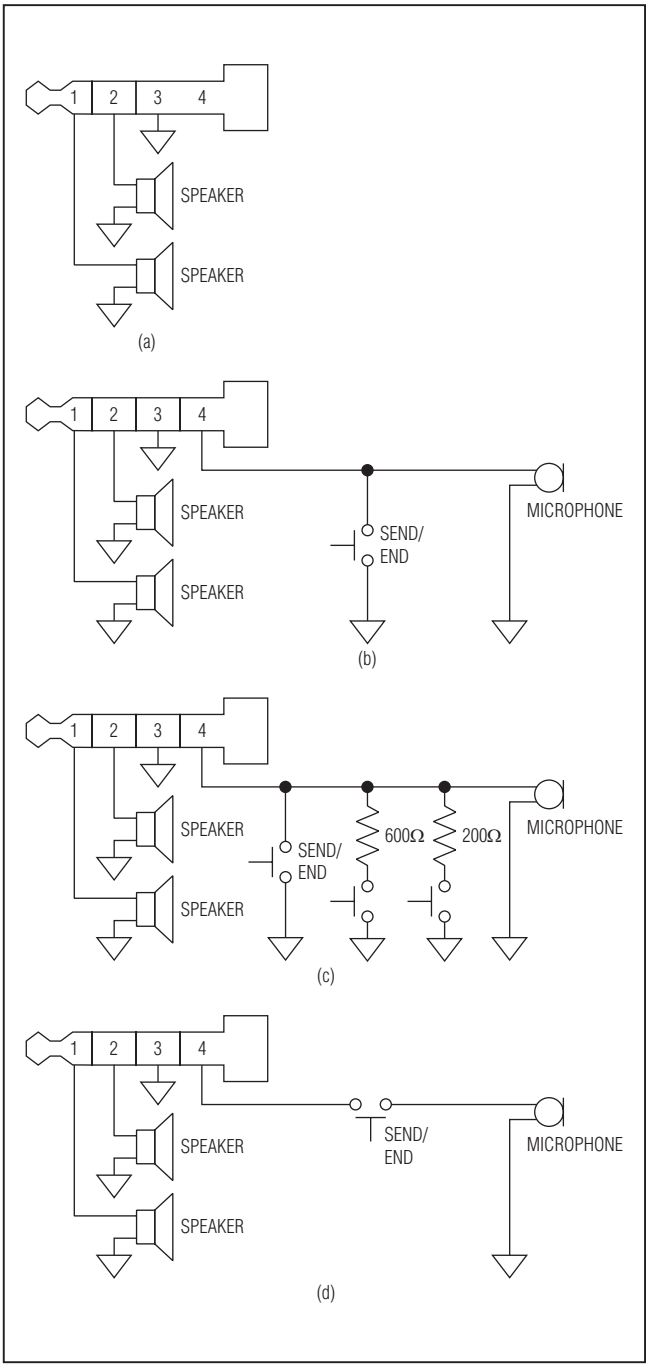
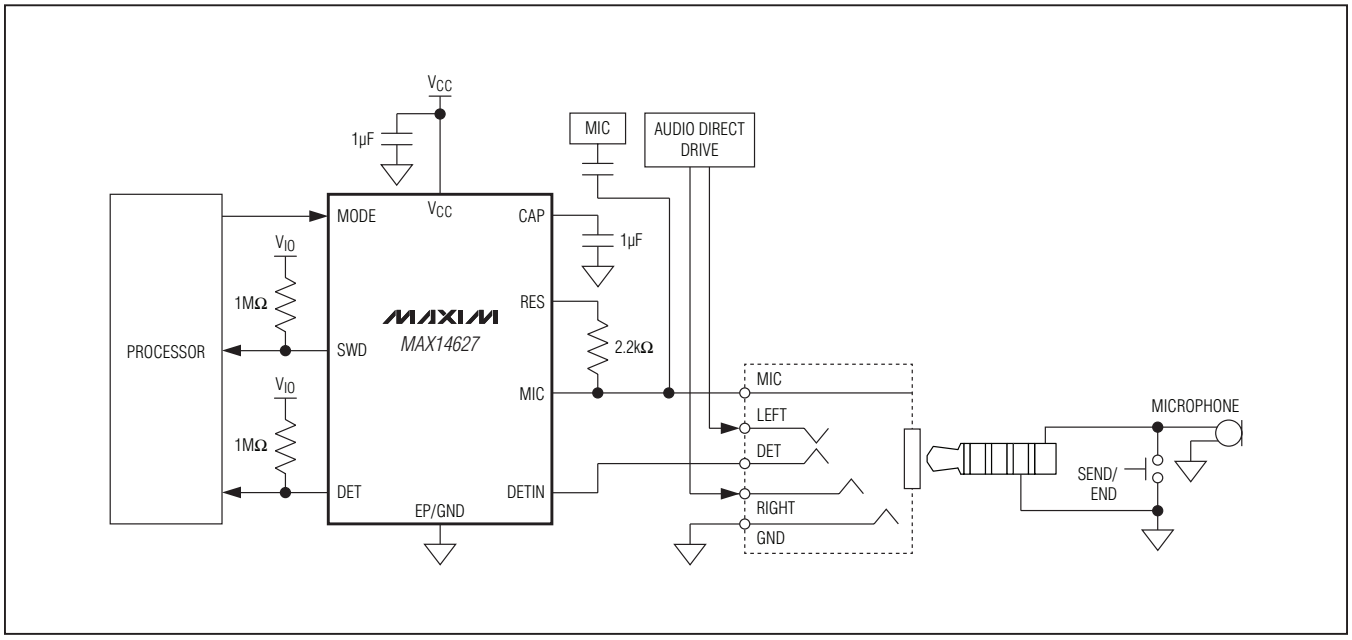


Figure 2. Supported 3.5mm Accessory Configurations

Typical Operating Circuits (continued)



Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX14627ETA+T	-40°C to +85°C	8 TDFN-EP*
MAX14628ETA+T	-40°C to +85°C	8 TDFN-EP*

+Denotes a lead(Pb)-free/RoHS-compliant package.
T = Tape and reel.
**EP = Exposed pad.*

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
8 TDFN-EP	T822+2	21-0168	90-0065

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	5/12	Initial release	—

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